

PSMN3R0-60ES

N-channel 60 V 3.0 m Ω standard level MOSFET in I2PAK.

Rev. 01 — 24 February 2011

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in a I2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

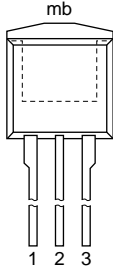
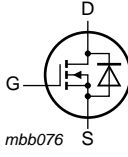
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	60	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1	[1]	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	306	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see Figure 11 ; see Figure 12	-	2.4	3	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 80\text{ A};$ $V_{DS} = 12\text{ V};$ see Figure 13 ; see Figure 14	-	28	-	nC

[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT226 (I2PAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R0-60ES	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

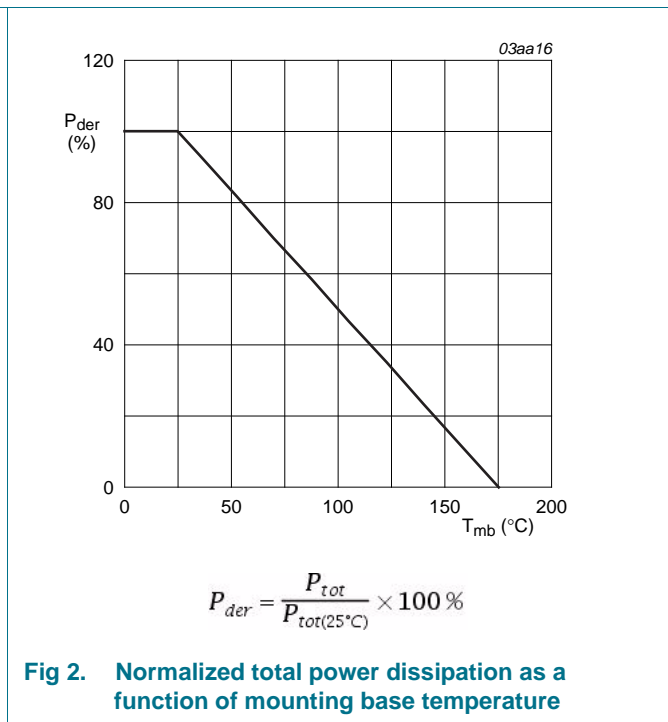
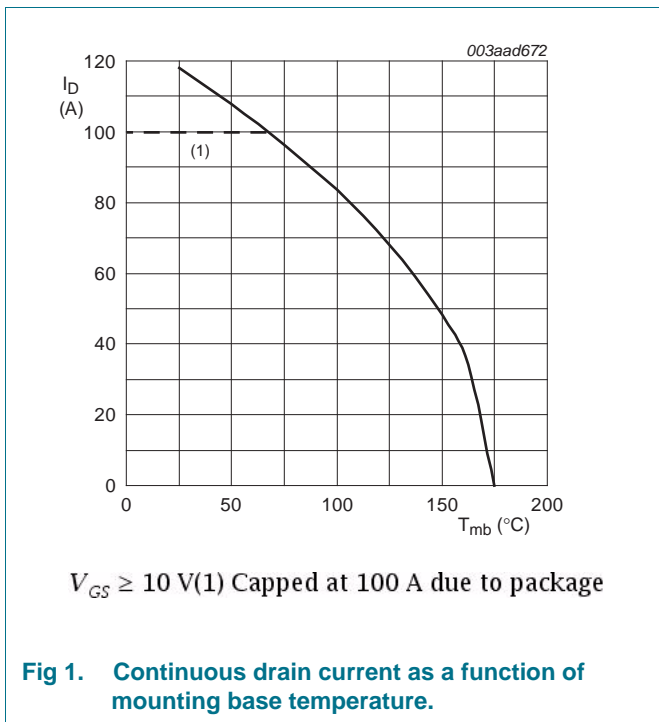
4. Limiting values

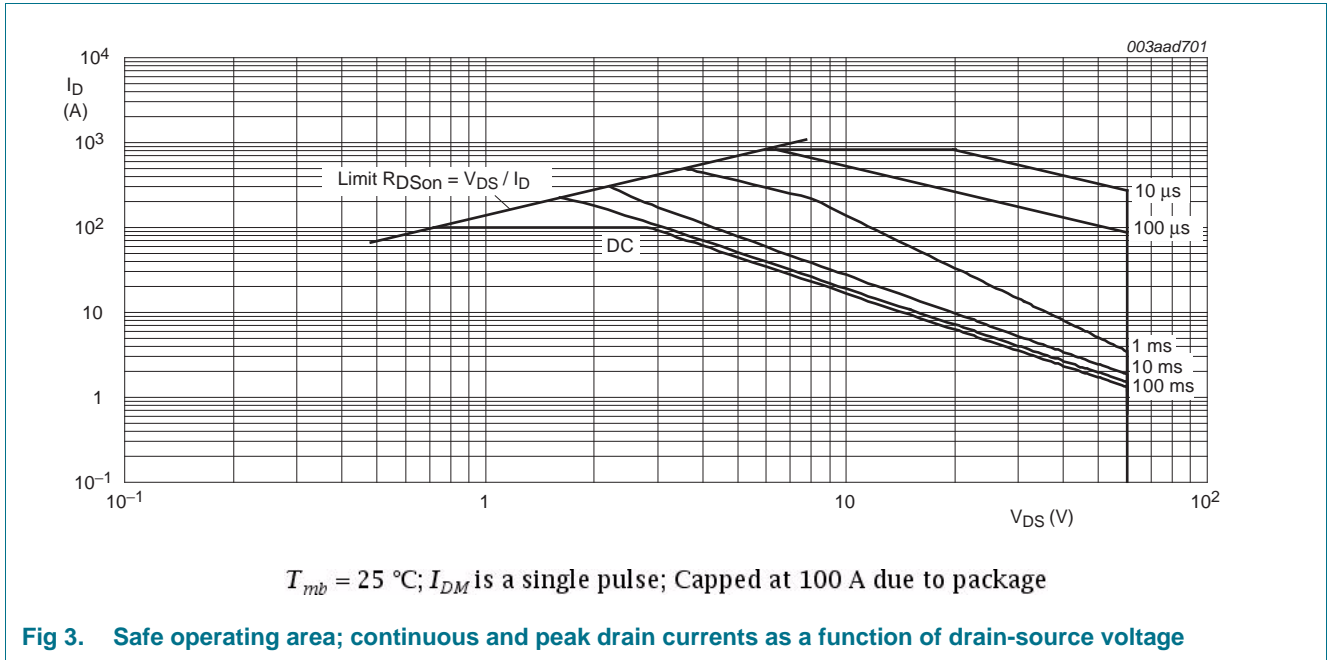
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	60	V
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	60	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1	-	83.4	A
		V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1	[1]	100	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; see Figure 3	-	824	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	306	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	[1]	100	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	824	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 100 A; V _{sup} ≤ 60 V; R _{GS} = 50 Ω; unclamped	-	800	mJ

[1] Continuous current is limited by package.

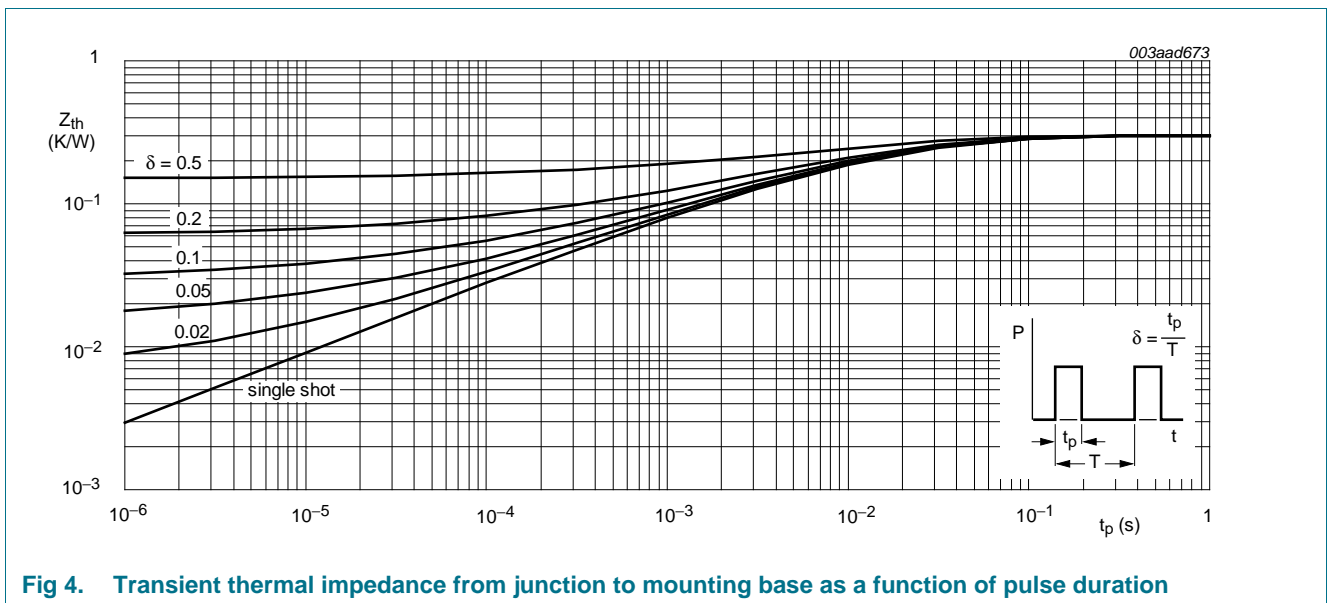




5. Thermal characteristics

Table 5. Thermal characteristics

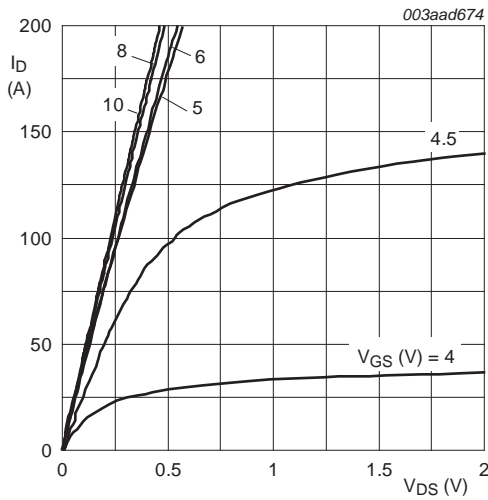
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.3	0.49	K/W



6. Characteristics

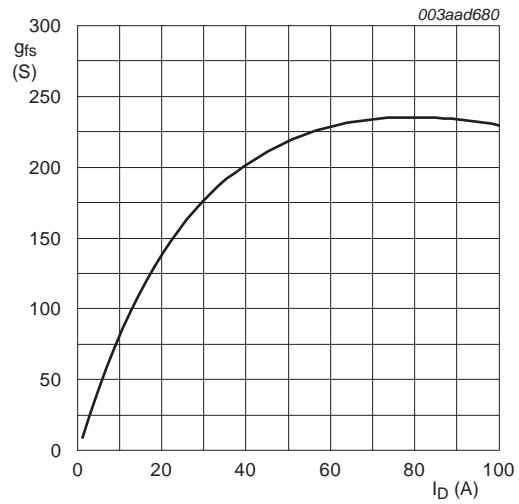
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ\text{C}$	54	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ\text{C}$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$; see Figure 8 ; see Figure 9	2	3	4	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C}$; see Figure 9	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$; see Figure 9	-	-	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	μA
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$; see Figure 10	-	-	7.2	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$; see Figure 11 ; see Figure 12	-	2.4	3	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	1.1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 80 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V}$; see Figure 13 ; see Figure 14	-	130	-	nC
Q_{GS}	gate-source charge	$I_D = 80 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V}$; see Figure 14 ; see Figure 13	-	43	-	nC
Q_{GD}	gate-drain charge	$I_D = 80 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V}$; see Figure 13 ; see Figure 14	-	28	-	nC
C_{iss}	input capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 15 ; see Figure 16	-	8079	-	pF
C_{oss}	output capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 15	-	971	-	pF
C_{rss}	reverse transfer capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$; see Figure 15 ; see Figure 16	-	492	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 0.5 \text{ } \Omega; V_{GS} = 10 \text{ V}$;	-	31	-	ns
t_r	rise time	$R_{G(ext)} = 1.5 \text{ } \Omega$	-	26	-	ns
$t_{d(off)}$	turn-off delay time		-	77	-	ns
t_f	fall time		-	22	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$; see Figure 17	-	0.88	1.2	V
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}$;	-	54	-	ns
Q_r	recovered charge	$V_{DS} = 30 \text{ V}$	-	97	-	nC



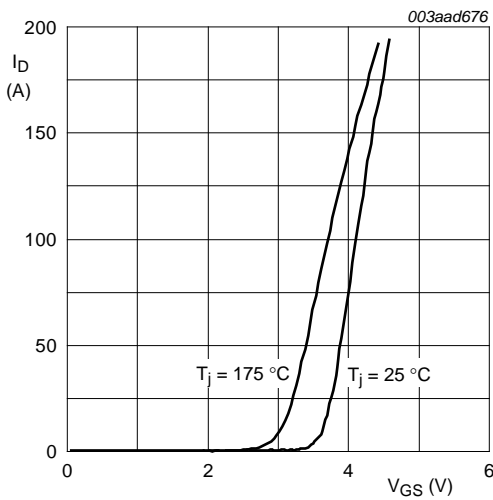
$T_j = 25\text{ }^\circ\text{C}; t_p = 300\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



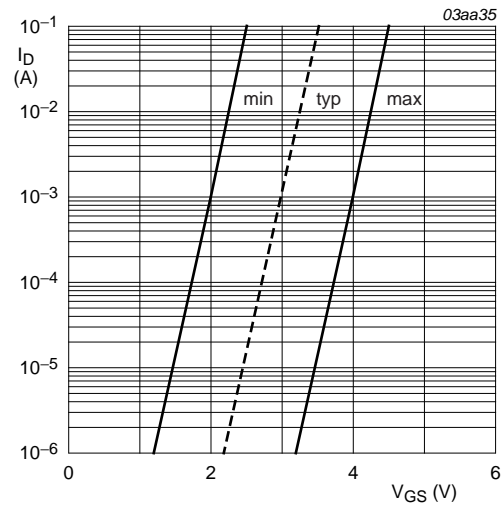
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 30\text{V}$

Fig 6. Forward transconductance as a function of drain current; typical values



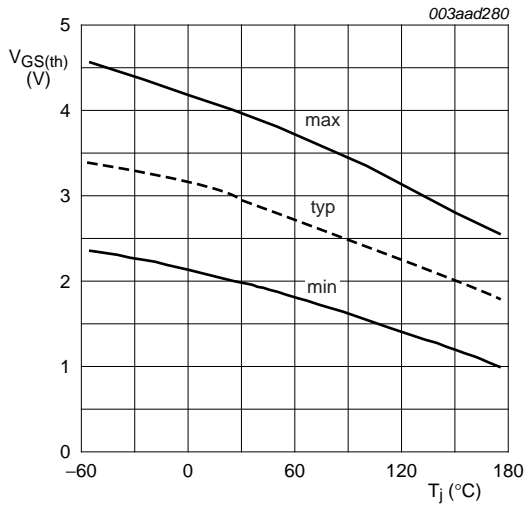
$V_{DS} = 30\text{V}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



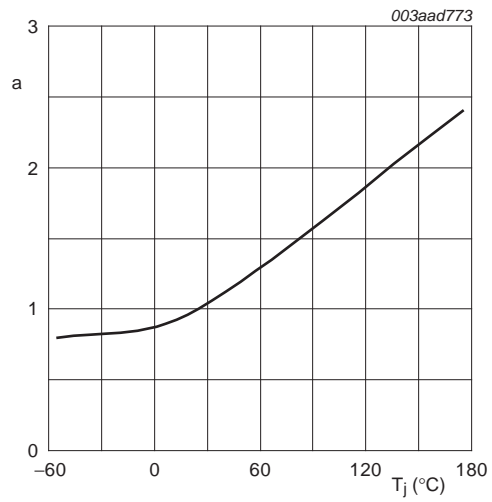
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



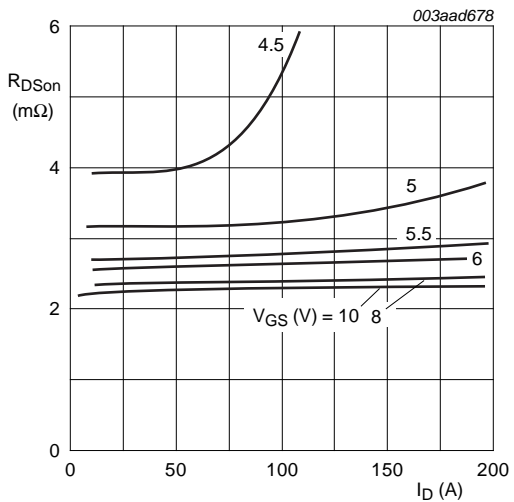
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



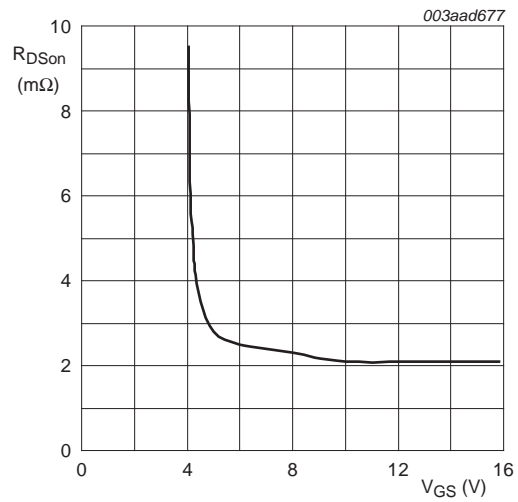
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



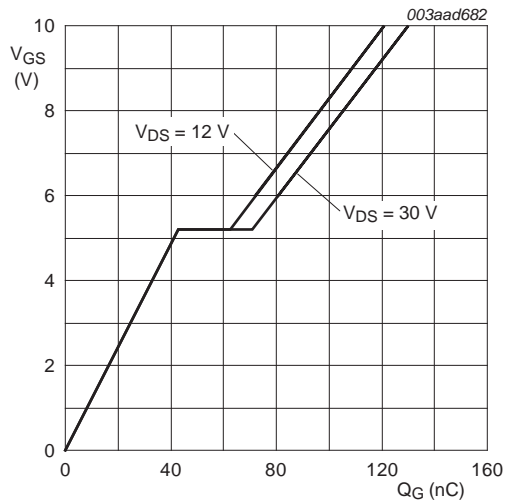
$T_j = 25 \text{ }^\circ\text{C}; t_p = 300 \text{ } \mu\text{s}$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values



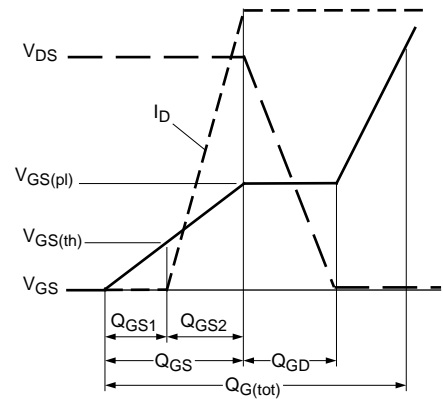
$T_j = 25 \text{ }^\circ\text{C}; I_D = 25 \text{ A}$

Fig 12. Drain-source on-state resistance as a function of gate-source voltage; typical values



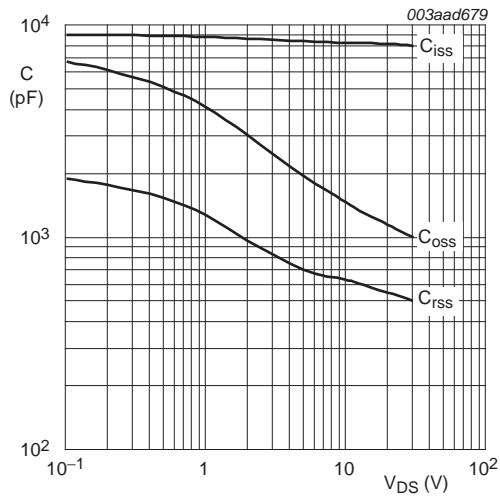
$T_j = 25\text{ }^\circ\text{C}; I_D = 80\text{ A}$

Fig 13. Gate-source voltage as a function of gate charge; typical values



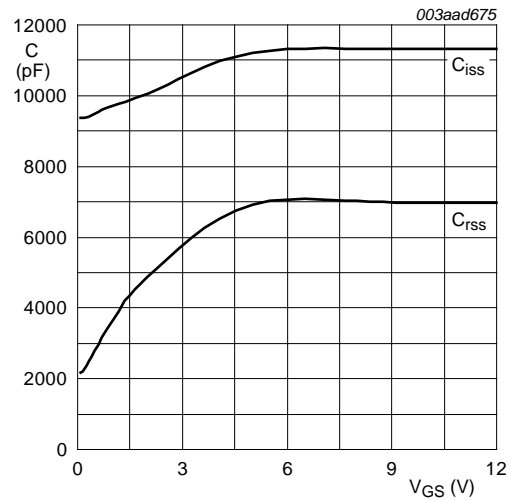
003aaa508

Fig 14. Gate charge waveform definitions



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$f = 1\text{ MHz}$

Fig 16. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

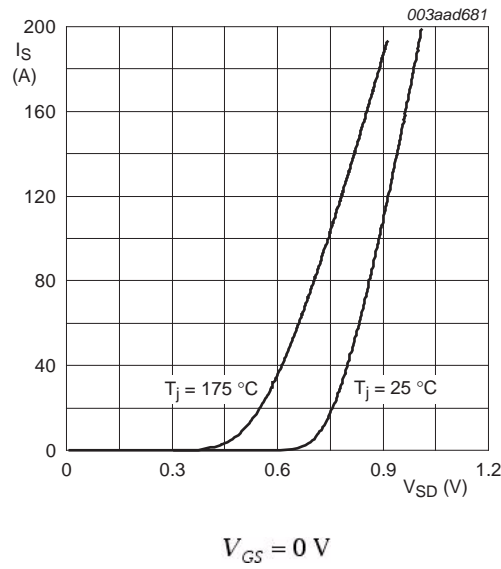


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended package (I2PAK); low-profile 3-lead TO-262

SOT226

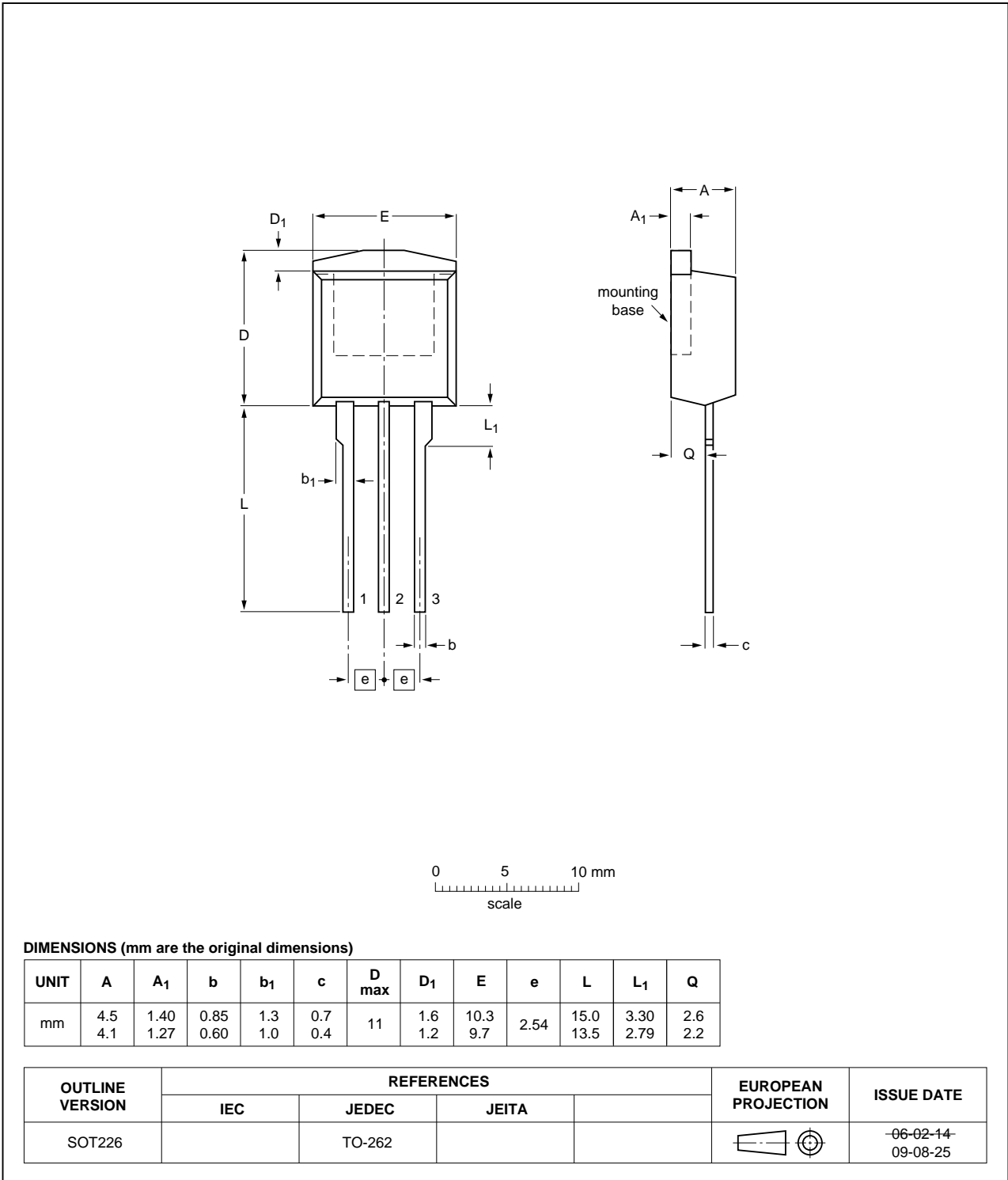


Fig 18. Package outline SOT226 (I2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN3R0-60ES v.1	20110224	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^[1] ^[2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	3
5	Thermal characteristics	4
6	Characteristics	5
7	Package outline	10
8	Revision history	11
9	Legal information	12
9.1	Data sheet status	12
9.2	Definitions	12
9.3	Disclaimers	12
9.4	Trademarks	13
10	Contact information	13

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